EXHIBIT J

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/327,944	07/10/2014	Keith Benson	ADHIT.029C1	5507

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EXAMINER
CHOE, HENRY

ART UNIT	PAPER NUMBER
2842	

NOTIFICATION DATE	DELIVERY MODE
09/09/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 14/327,944	Applicant(s) BENSON, KEITH	
	Examiner HENRY CHOE	Art Unit 2842	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/28/15*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *17-36* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *17-20,24-31,33,35 and 36* is/are rejected.

8)☒ Claim(s) *21-23, 32 and 34* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-20, 24-31, 33, 35 and 36 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Chick (Fig. 3A) in view of Banba (Fig. 23).

Regarding claims 17, 19 and 31, Chick (Fig. 3A) discloses an amplifier circuit comprising an input transmission line [TLIN, TLI11, 12, TLI12, 13, TLI1(N-1), 1N], an output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN), and a plurality of cascode amplifiers (1st cascode amplifier: Q11, Q21, QM1; 2nd cascode amplifier: Q12, Q22, QM2; 3rd cascode amplifier: Q1N, Q2N, QMN) and each coupled between the input transmission line [TLIN, TLI11, 12, TLI12, 13, TLI1(N-1), 1N] and the output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN) and wherein a first cascode amplifier (Q11, Q21, QM1) of the plurality of cascode amplifiers (1st cascode amplifier: Q11, Q21, QM1; 2nd cascode amplifier: Q12, Q22, QM2; 3rd cascode amplifier: Q1N, Q2N, QMN) comprises three or more FETs (Q11, Q21, QM1) arranged in a stack and wherein the three or more FETs (Q11, Q21, QM1) comprises a first FET (Q11) and a second FET (Q21) and a third FET (QM1) and wherein the first FET (Q11) includes a gate (gate terminal of Q11) coupled to the input transmission line [TLIN, TLI11, 12, TLI12, 13, TLI1(N-1), 1N] and wherein the second FET (Q21) is position between the first FET (Q11) and the third FET (QM1) in the stack and wherein the third FET (QM1) includes a drain (drain terminal of QM1) coupled to the output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN). As described above, Chick (Fig. 3A) discloses all the limitations in claim 1 except for that the first

stabilization circuit coupled to the drain of the third FET. Banba (Fig. 23) discloses an amplifier circuit comprising the first stabilization circuit (Rf, Cf) coupled to the drain of the FET (M2). It would have been obvious to one of ordinary skill in the art, at the time the invention was made would have found it obvious to have employed the first stabilization circuit (Rf, Cf) at the drain terminal of the third FET of Chick (Fig. 3A), such as taught by Banba (Fig. 23) in order to provide the advantageous benefit of stabilizing the variation of the gain of the amplifier.

Regarding claims 18 and 28, wherein the first stabilization circuit (Rf, Cf) comprises a first resistor (Rf) and a first capacitor (Cf) electrically connected in series.

Regarding claim 20, Banba (Fig. 23) further comprising a second stabilization circuit (RL, LL) coupled to a drain (drain terminal of M4) of the FET (M4).

Regarding claims 24, 30 and 36, Chick (Fig. 3A) further comprising a gate line termination (R1N) coupled to the input transmission line [TLIN, TLI11, 12, TLI12, 13, TLI1(N-1), 1N] and a drain line termination [Chick (Fig. 3A) inherently includes a termination resistor since it would not work without it] coupled to the output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN).

Regarding claim 25, wherein the first stabilization circuit (Rf, Cf) is configured to inhibit parametric oscillations.

Regarding claim 26, wherein the plurality of cascode amplifiers (1st cascode amplifier: Q11, Q21, QM1; 2nd cascode amplifier: Q12, Q22, QM2; 3rd cascode amplifier: Q1N, Q2N, QMN) comprises between four and ten cascode amplifiers.

Regarding claims 27 and 29, Chick (Fig. 3A) discloses an amplifier circuit comprising an input transmission line [TLIN, TLI11, 12, TLI12, 13, TLI1(N-1), 1N], an output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN), and a plurality of cascode amplifiers (1st cascode amplifier: Q11, Q21, QM1; 2nd cascode amplifier: Q12, Q22, QM2; 3rd cascode amplifier: Q1N, Q2N, QMN) and each coupled between the input transmission line [TLIN, TLI11, 12, TLI12, 13,

TLI1(N-1), 1N] and the output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN) and wherein a first cascode amplifier (Q11, Q21, QM1) of the plurality of cascode amplifiers (1st cascode amplifier: Q11, Q21, QM1; 2nd cascode amplifier: Q12, Q22, QM2; 3rd cascode amplifier: Q1N, Q2N, QMN) comprises three or more FETs (Q11, Q21, QM1) arranged in a stack and wherein the three or more FETs (Q11, Q21, QM1) comprises a first FET (Q11) and a second FET (Q21) and a third FET (QM1) and wherein the first FET (Q11) includes a gate (gate terminal of Q11) coupled to the input transmission line [TLIN, TLI11, 12, TLI12, 13, TLI1(N-1), 1N] and wherein the second FET (Q21) is position between the first FET (Q11) and the third FET (QM1) in the stack and wherein the third FET (QM1) includes a drain (drain terminal of QM1) coupled to the output transmission line [TLO11, 12, TLO13, 14, TLO1(N-1), 1N, TLO1N, 2N, TLO2(N-1), 2N, TLO23, 24, TLO21, 22, TLO21, 31, TLO(M-1)1, M1, TLOM1, M2, TLOM3, M4, TLO(M-1)N, MN). As described above, Chick (Fig. 3A) discloses all the limitations in claim 1 except for that the first stabilization circuit coupled to the drain of the second FET. Banba (Fig. 23) discloses an amplifier circuit comprising the first stabilization circuit (Rf, Cf) coupled to the drain of the FET (M2). It would have been obvious to one of ordinary skill in the art, at the time the invention was made would have found it obvious to have employed the first stabilization circuit (Rf, Cf) at the drain terminal of the second FET of Chick (Fig. 3A), such as taught by Banba (Fig. 23) in order to provide the advantageous benefit of stabilizing the variation of the gain of the amplifier.

Regarding claim 33, Chick (Fig. 3A) further comprising a second stabilization circuit (Q11RM1) coupled to a gate (gate terminal of Q21) of the second FET (Q21).

Regarding claim 35, furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented the specific range of the resistance value for the first resistor, since they are based on the routine experimentation to obtain the optimum operating parameters.

Allowable Subject Matter

Claims 21-23, 32 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

/HENRY CHOE/

Primary Examiner, Art Unit 2842